CLAIMS

What is claimed is:

1. A magnetic memory cell, comprising:

a first ferromagnetic layer;

a second ferromagnetic layer; and

an insulating layer disposed between the first and second ferromagnetic layers, the insulating layer in combination with the first and second ferromagnetic layers forming a diode such that leakage currents are prevented.

2. The magnetic memory cell as set forth in claim 1, wherein:

the second ferromagnetic layer is disposed on a bottom conductor line;

the bottom conductor line is disposed on a substrate; and

a top conductor line is disposed on the first ferromagnetic layer.

3. A memory cell array comprising a plurality of the magnetic memory cells of claim 2.

4. The memory cell array as set forth in claim 3, wherein the diodes prevent leakage currents between adjacent cells of the memory cell array.

5. The magnetic memory cell as set forth in claim 1, wherein the insulating layer is formed from the group consisting of:

aluminum oxide;

hafnium oxide; and

zirconium oxide.

6. The magnetic memory cell as set forth in claim 1, wherein the first ferromagnetic layer is formed from iron-cobalt.

7. The magnetic memory cell as set forth in claim 1, wherein the second ferromagnetic layer is formed from nickel-iron.

8. A method of reading a memory structure, comprising:

generating a first current during a first read cycle, the first current flowing from a column line through the memory structure to a row line; and

generating a second current during a second read cycle, the second current flowing from the row line through the memory structure to the column line.

9. The method of reading a memory structure as set forth in claim 8, wherein the direction of current flow through the memory structure is reversed for each subsequent read cycle.

10. The method of reading a memory structure as set forth in claim 9, wherein the memory structure comprises:

a free magnetic layer;

a pinned magnetic layer; and

an insulating layer disposed between the free and pinned magnetic layers.

11. The method of reading a memory structure as set forth in claim 9, wherein the reversal of the direction of current flow during read cycles extends a storage life of the memory structure.

12. The method of reading a memory structure as set forth in claim 8, wherein the memory structure comprises:

a free magnetic layer;

a pinned magnetic layer; and

an insulating layer disposed between the free and pinned magnetic layers.

13. A memory cell, comprising:

a fixed magnetic layer having a magnetic moment that is fixed in a pre-determined direction;

a free magnetic layer having a magnetic moment that is free to rotate under an influence of an applied magnetic field; and

an insulating layer disposed between the fixed and free magnetic layers;

wherein the insulating layer in combination with the fixed and free magnetic layers form a tunneling diode, the tunneling diode allowing a current between the free magnetic layer when selected and the fixed magnetic layer when selected but blocking leakage currents between the fixed magnetic layer when not selected and the free magnetic layer when not selected.

14. A memory cell array comprising a plurality of the memory cells of claim 13, the memory cells being interconnected by a plurality of column conductor lines and row conductor lines with memory cell being disposed at junctions of the column conductor lines and the row conductor lines.

15. The memory cell as set forth in claim 14, wherein the column conductor lines are connected to the free magnetic layers and the row conductor lines are connected to the fixed magnetic layers.

16. The memory cell as set forth in claim 15, wherein the column conductor lines and the row conductor lines are connected to a decoder and sense amplifier at each of their respective ends.

17. The memory cell as set forth in claim 13, wherein the insulating layer is formed from the group consisting of aluminum oxide, hafnium oxide and zirconium oxide.

18. The memory cell as set forth in claim 13, wherein the tunnel diode prevents leakage currents from flowing between adjacent memory cells during a read cycle.

19. A method of reading an array of memory cells, comprising:

providing a plurality of column lines and row lines connected across the array of memory cells;

selecting a column line;

selecting a row line during a first read cycle such that a first current flows from the column line through a first memory cell to the row line; and

reversing the current flow during a second read cycle of the first memory cell such that the storage life of the memory cell is extended.

20. The method as set forth in claim 19, wherein a direction of the current flow through the first memory cell is reversed for each subsequent read cycle.

21. The method as set forth in claim 19, wherein the current flows from the row line to the column line during the second read cycle.

22. The method as set forth in claim 19, wherein the number of read cycles is recorded for each memory cell in the array.